IN THE CLAIMS

1-15. (Canceled)

16. (Previously presented) A apparatus comprising:

a first transistor to receive and amplify an RF signal and output a first signal;

a second transistor to receive and amplify the RF signal, wherein the second transistor is physically smaller than the first transistor; and

a circuit to receive an RF signal amplified by the second transistor and to output a second signal proportional to the first signal.

17. (Previously presented) The apparatus of claim 16, wherein the circuit comprises a resistor element.

18. (Previously presented) The apparatus of claim 16, further comprising a bias network to establish an operating point for the first transistor.

19. (Previously presented) The apparatus of claim 18, wherein the bias network is configured to establish an operating point for the second transistor.

20. (Previously presented) The apparatus of claim 16, wherein said circuit generates a sense voltage proportional to power of said first transistor.

21. (Previously presented) The apparatus of claim 16, wherein said first transistor comprises a first field-effect transistor, and said second transistor comprises a second field-effect transistor.

22. (Previously presented) The apparatus of claim 21, wherein said first signal corresponds to a drain output of said first field-effect transistor, and said second signal corresponds to a drain output of said second field-effect transistor.

23. (Previously presented) The apparatus of claim 22, wherein said circuit comprises a resistor element coupled to a drain of said second field-effect transistor.

24. (Previously presented) The apparatus of claim 23, wherein a gate of said first field-effect transistor is coupled to a gate of said second field-effect transistor.

25. (Previously presented) The apparatus of claim 24, wherein said RF signal is applied to said gate of said first field-effect transistor and is applied to said gate of said second field-effect transistor.

26. (Previously presented) A system for sensing RF amplifier output power comprising:

a RF amplifier transistor configured to receive and amplify a RF signal;

a sampling transistor configured to receive and amplify a RF signal, wherein the sampling transistor is physically smaller than the RF amplifier transistor such that the sampling transistor is capable of producing a proportionally smaller amplified RF signal than that capable of being produced by the RF amplifier transistor for a RF input signal common to both the RF amplifier transistor and the sampling transistor; and

a current sensing circuit configured to receive a RF signal amplified by the sampling transistor and generate a

current proportional to a RF signal amplified by the RF amplifier transistor.

27. (Previously presented) The system according to claim 26, further including a bias network configured to establish a quiescent operating point for the RF amplifier transistor.

28. (Previously presented) The system according to claim 27, wherein the bias network is further configured to establish a quiescent operating point for the sampling transistor, by associating a first bias resistor with the sampling transistor.

29. (Previously presented) The system according to claim 28, wherein the bias network comprises a second bias resistor associated with the RF amplifier transistor.

30. (Previously presented) The system according to claim 29, wherein said first bias resistor and said second bias resistor are the same resistor.

31. (Previously presented) The system according to claim 26, further comprising a first RF signal coupling capacitor

configured to pass the RF signal to the RF amplifier transistor.

32. (Previously presented) The system according to claim 31, further comprising a second RF signal coupling capacitor configured to pass the RF signal to the sampling transistor.

33. (Previously presented) The system according to claim 32, wherein said first RF signal coupling capacitor and the second RF signal coupling capacitor are the same capacitor.

34. (Previously presented) A system for sensing RF amplifier output power comprising:

means for amplifying a RF input signal and generating a RF output signal therefrom;

means for sampling a RF input signal that is associated with both the amplifying means and the sampling means and generating a sampled signal therefrom; and

means for sensing the sampled signal and generating a current sensing signal therefrom proportional to a power amplitude associated with the RF output signal.

35. (Previously presented) The system according to claim 34, further comprising biasing means for biasing the sampling means and further for biasing the amplifying means such that a bias current associated with the sampling means is proportional to a bias current associated with the amplifying means.

36. (Previously presented) The system according to claim 35, wherein the amplifying means comprises a first transistor.

37. (Previously presented) The system according to claim 36, wherein said means for sampling comprises a second transistor, and said second transistor is physically smaller than said first transistor.

38. (Previously presented) A system for sensing RF amplifier output power comprising:

a first amplifying transistor device to amplify a RF input signal and generate a RF output signal therefrom;

a second amplifying transistor device to sample a RF input signal that is associated with both the first amplifying transistor device and the second amplifying transistor device and generate a sampled signal therefrom; and

means for sensing the sampled signal and generating a current sensing signal therefrom proportional to a power amplitude associated with the RF output signal.

39. (Previously presented) The system of claim 38, wherein said second amplifying transistor device is physically smaller than said first amplifying transistor device.

40. (Previously presented) The system of claim 39, further comprising biasing means for biasing the second amplifying transistor device and further for biasing the first amplifying transistor device such that a bias current associated with the second amplifying transistor device is proportional to a bias current associated with the first amplifying transistor device.

41. (Previously presented) A method for sensing RF signal power amplitude, the method comprising the steps of:

(a) providing a RF signal amplifier comprising a first transistor having a first predetermined size;

(b) providing a sampling amplifier comprising a second transistor having a second predetermined size that is smaller than the first predetermined size;

(c) amplifying a RF input signal to produce a first RF output signal; and

(d) sampling the RF input signal to produce a second RF output signal proportional to the first RF output signal, wherein the proportion is associated with a ratio determined by the first and second predetermined sizes.

42. (Previously presented) The method of claim 41, further comprising the step of:

(e) converting the second RF output signal to a current sensing signal such that the current sensing signal is proportional to a power amplitude associated with the first RF output signal.

43. (Previously presented) A system for sensing RF amplifier output power comprising:

a RF amplifier transistor configured to receive and amplify a RF signal;

a sampling transistor configured to receive and amplify a RF signal, wherein the sampling transistor is physically smaller than the RF amplifier transistor such that the sampling transistor is capable of producing a proportionally smaller amplified RF signal than that capable

of being produced by the RF amplifier transistor for a RF input signal common to both the RF amplifier transistor and the sampling transistor;

a current sensing circuit configured to receive a RF signal amplified by the sampling transistor and generate a current proportional to a power amplitude associated with the RF signal amplified by the RF amplifier transistor; and

a bias circuit configured to establish quiescent operating characteristics associated with the RF amplifier transistor and the sampling transistor, the bias circuit comprising a first bias resistor associated with the RF amplifier transistor and further comprising a second bias resistor associated with the sampling transistor.

44. (Previously presented) Amplifier circuitry comprising:

a) a radio frequency power amplifier for amplifying a radio frequency input signal and having:

i) a radio frequency amplifier input for receiving the radio frequency input signal,

ii) a bias input for receiving a bias signal for biasing the radio frequency power amplifier, and

iii) a power amplifier output providing an amplified radio frequency signal;

b) a first transistor circuit having:

i) a first input for receiving the radio frequency input signal,

ii) a first bias input for receiving the bias signal, and

iii) a first output providing a first output signal having a bias component and a radio frequency component proportionally smaller than the amplified radio frequency signal; and

c) bias circuitry adapted to provide the bias signal as a function of the first output, wherein the bias circuitry provides the bias signal to compensate for output power of the amplified radio frequency signal.

45. (Previously presented) The amplifier circuitry of claim 44, wherein the radio frequency power amplifier is implemented using transistor circuitry.

46. (Previously presented) Amplifier circuitry comprising:

a) a radio frequency power amplifier for amplifying a radio frequency input signal and having:

i) a radio frequency amplifier input for receiving the radio frequency input signal,

ii) a bias input for receiving a bias signal for biasing the radio frequency power amplifier, and

iii) a power amplifier output providing an amplified radio frequency signal;

b) a first transistor circuit having:

i) a first input for receiving the radio frequency input signal,

ii) a first bias input for receiving the bias signal, and

iii) a first output providing a first output signal having a bias component and a radio frequency component proportionally smaller than the amplified radio frequency signal; and

c) bias circuitry adapted to provide the bias signal as a function of the first output, wherein the bias circuitry provides the bias signal based on output power of the amplified radio frequency signal.

47. (Previously presented) The amplifier circuitry of claim 46, wherein the radio frequency power amplifier is implemented using transistor circuitry.

48. (Previously presented) A power amplifying circuit comprising:

an amplifying transistor which receives an input signal; and

a sense transistor being smaller in size than the output transistor, the sense transistor receiving said input signal,

wherein an output current of the sense transistor is proportional to an output current of the output transistor.

49. (Previously presented) A power amplifying circuit comprising:

a first transistor which receives an input signal and generates an output;

a second transistor being smaller in size than the first transistor, the second transistor also receiving said input signal; and

a resistor element coupled to the second transistor, wherein a voltage formed across the resistor element is proportional to the output of the first transistor.

50. (New) A system for sensing RF amplifier output power comprising:

a RF amplifier having an amplifier transistor and further having a first RF signal input port and a first RF signal output port;

a sampling amplifier having a sampling transistor, a second RF signal input port coupled to the first RF signal input port and further having a second RF signal output port, wherein the sampling transistor is physically smaller than the amplifier transistor; and

a current sensing network being operatively connected to said second RF signal output port, wherein said current sensing network has a bias input port.

51. (New) The system according to claim 50, wherein the current sensing network comprises a resistor coupled at one end to the second RF signal output port and coupled at an opposite end to the bias input port.

52. (New) The system according to claim 51, wherein the current sensing network further comprises a capacitor coupled at one end to the second RF signal output port and coupled at an opposite end to a signal ground point associated with the system.

53. (New) The system according to claim 52 further comprising a bias network.

54. (New) The system according to claim 53 further comprising a first bias resistor coupled at one end to the amplifier transistor and coupled at an opposite end to the bias network.

55. (New) The system according to claim 54 further comprising a second bias resistor coupled at one end to the sampling transistor and coupled at an opposite end to the bias network.

56. (New) The system according to claim 51, wherein the current sensing network further comprises a capacitor coupled at one end to the second RF signal output port and coupled at

b1 an opposite end to a reference potential point associated with the system.